Principles of Testing Electronic Systems

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Definition

Testing is the process to determine whether a piece of equipment:
- is functioning correctly
- is defective (broken or faulty).

Equipment can be defective because it doesn't function:
- as designed
- as specified.

A part fails to operate properly:
- design doesn't correspond to specification
  - logic design incorrect
  - physical design incorrect
- physical part doesn't correspond to design
  - manufacturing defect present
  - wear out defect present

- external or environmental disturbance:
  - transient disturbance
  - power or temperature specification violated

Reliability and Testing

Reliability of *electronics systems* is no longer limited to military, aerospace and banking:
- They are ubiquitous in the workplace
- Used by almost everyone
- Made of smaller and smaller devices
- Have continually new failure modes
- Reliability depending on being error free
- Failures in both software and hardware

Here we concentrate on hardware

Verification and Testing

Testing a circuit prior to fabrication is known as *design verification.*

Verification is certainly done at various stages of the design process as shown before.

Most viable design verification is simulation although formal verification is increasingly used.

Testing is identifying that the fabricated circuit is free from errors.

Need to specify what *errors* testing a looking for.

Faults and their Detection

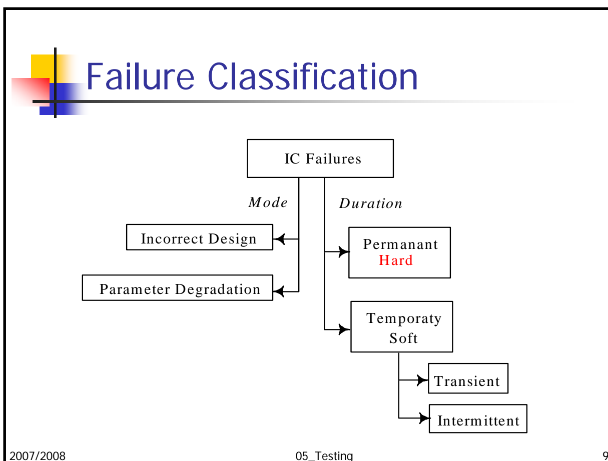
Physical failures are manifested as electrical failure and are interpreted as *faults* on the logic level.

Several physical defects may be mapped into fewer or even one fault type.

The mail fault used in digital circuit is the infamous *Stuck-at Fault.*

A fault is detected by a test pattern, i.e. an input combination that confirm the presence of the fault

Failure Classification



Hard Vs Soft Failures

Hard failure:	Permanent	
Soft failure:	Temporary	
▪ Transient	>>	External Factors
▪ Intermittent	>>	Wearout

Physical Defects

Metalization and metal semiconductor
- Open metal at oxide steps
- Wire bonding failure
- Inter-metallic compound formation
- Electromigration

Surface and bulk effect
- Passivation pits and cracks
- Gate oxide breakdown
  - Pinholes or thin spots in oxide
  - Electrical over-stress
- Surface potential instability

Failure Modes

On the electrical level
- Most physical defects results into
  - Opens
  - Shorts

Effect of an open:
- technology dependent
- not strictly high-Z behavior

Effect of a short:
- a solid short represented by 0 resistance
- but mostly is resistive

Fault Models

Fault Model	Description
Single Stuck-at Faults (SSA)	One line takes the value 0 or 1.
Multiple Stuck-at Faults	Two or more lines have fixed values, not necessarily the same.
Bridging Faults	Two or more lines that are normally independent become electrically connected
Stuck-Open Faults (SOP)	A failure in a pull-up or pull-down transistor in a CMOS logic causes it to behave as a memory element

Fault Model	Description
Stuck-On Faults (SON)	A transistor is always conducting.
Delay Faults	A fault is caused by delays in one or more paths in the circuit.
Intermittent Faults	Caused by internal parameter degradation. Incorrect signal values occur for some but not all states of the circuit. Degradation is progressive until permanent failure occurs
Transient Faults	Incorrect signal values caused by coupled disturbance. Coupling may be via power bus capacitive or inductive coupling. Includes both internal and external sources as well as particle irradiation.

SA Faults: Example 1


```
Inputs     FF          Faulty Response
AB      Response    A/0 B/0 Z/0 A/1 B/1 Z/1
-----------------------------------------------
00         0         0   0   0   0   0   1
01         0         0   0   0   1   0   1
10         0         0   0   0   0   1   1
11         1         0   0   0   1   1   1
-----------------------------------------------
```


SA Faults: Example 2

Inpu	Response						
SAB	FF	S/0	S/1	C/0	C/1	D/0	D/1
000	0	0	0	0	0	0	0
001	1	1	**0**	1	1	1	**0**
010	0	0	**1**	0	**1**	0	0
011	1	1	1	1	1	1	**0**
100	0	0	0	0	0	0	0
101	0	**1**	0	0	0	**1**	0
110	1	**0**	1	**0**	1	1	1
111	1	1	1	**0**	1	1	1

Fault Properties

Given F1 and F2 with T1 and T2

Equivalence:

- F1 is equivalent to F2 if T1 = T2
- Any test detecting F1, detects F2 and vice versa

Dominance:

- F1 dominates F2 if T2 $\subseteq$ T1
- a test detecting F2 detects also F1
- the relation is not symmetric

Fault Collapsing

1 {A/0, B/0, H/0}
2 {C/1, D/1, F/1, G/0}
3 {E/0, G/0, V/0}
4 {H/1, V/1, Z/1}
5 {F/0, G/1}
6 A/1 $\rightarrow$ H/1, thus A/1 can represent H/1 and all its equivalent faults in class 4
7 C/0 $\rightarrow$ F/0, thus C/0 can represent F/0 and all its equivalent faults in class 5
8 V/0 $\rightarrow$ Z/0, but V/0 belongs to equivalence class 3, which has been merged into class 2.
Any fault from this class is dominated by Z/0.
9 B/1 $\rightarrow$ H/1
10 D/0 $\rightarrow$ F/0
11 E/1 $\rightarrow$ V/1

{A/0, A/1, B/1, C/0, C/1, D/0, E/1}

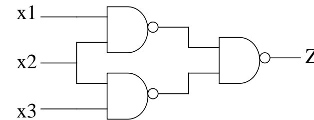
Fault detection

Definition:
A test vector t detects a fault **t** iff Z_f (t) ≠ Z(t), i.e. Z(t) ⊕ Z_f (t) = 1

Z(x) - logic function of the circuit
Z_f - logic function of the circuit when fault f is there

Example

Consider fault α= x2 SA1
- find Z , Z_α
- check if (101) detects Z_α



Z = [(x1 x2)′(x2 x3)′]′
= x1 x2 +x2 x3
= x2 (x1 + x3)
α= x2 SA1
Z ⊕ Z_α | (1,0,1) = Z ⊕(x1+x3)=0 ⊕ 1 =1

Fault coverage

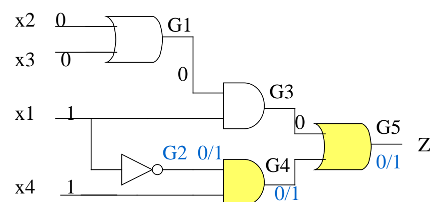
If only **f** out of **x** faults have been detected by a test then "test coverage " is **tc = f/x** ≤ **1**

Path sensitization

A line whose value changes in the presence of the fault is **sensitized** to the fault by the test **t**.
A path composed of sensitized lines is called a **sensitized path**.

Example

Consider G2 SA1



Path sensitization algorithm

I. specify inputs to generate at the site of the fault.
II. propagate error to the output
III. specify inputs to obtain signal values needed in II

Detectability

If no test can detect fault **f** => **f** is **undetectable** such a circuit is **redundant.**

An undetectable fault can prevent detection of another fault.

Example

b SA0 is detected by t =1101

A=1
a = 0
0
1
C=0
D=1
0
1
0/1
B=1
0/1
b=1/0
1/0

b SA0 is **no longer detected** by t =1101 if a SA1 is present

A=1
a=0/1
0/1
1/0
C=0
D=1
0
1
0
B=1
0/1
b=1/0
1/0

Redundancy removal

Redundant circuit can always be **simplified** by removing a gate or gate input

Rules

Undecetectable fault	simplification rule
AND (NAND) input sa1	remove input
AND (NAND) input sa0	remove gate, replace by 0(1)
OR (NOR) input sa0	remove input
OR (NOR) input sa1	remove gate, replace by 1(0)

Redundancy may be used to **avoid hazards**
Example: consider : b=c=1, a changes from 1 to 0

a=1u0
b=111
X=1u0
redundant
Y
c=111
F= ab + a'c
= 1u1
Z=0u1

Test Pattern Generation

NP-complete problem

Methods:

- Algebraic: Boolean Difference
- General Fault Objective: Critical Path
- Algorithmic: D-Algorithm Roth 1967 IBM

Boolean difference w.r.t. a primary input

Definition: the Boolean difference of f(x) is equal $D(f) = df(x)/dx = f(x) \oplus f(x')$

An equivalent definition results from the Shannon's law $f(x) = x\,f(1) + x'\,f(0)$

Lemma: $f(x) \oplus f(x') = f(0) \oplus f(1)$

Then the Boolean difference is

$$f(x_1,\dots,x_i=0,\dots,x_n) \oplus f(x_1,\dots,x_i=1,\dots,x_n) = 1$$

Boolean difference can be used to obtain all tests for stuck-at faults

x sa0 will be tested by input vectors that satisfy :

$T_0 = x\,(df/dx) = 1$

x sa1 will be tested by

$T_1 = x'(df/dx) = 1$

Example 1

Let us consider $f(x) = x_1x_2 + x_3$

$df(x)/dx_2 = x_3 \oplus (x_1 + x_3) = x_3'x_1 = 1$. Then

$x_1 = 1$ and $x_3 = 0$.

For the SA1 and SA0 faults on x_2, the patterns are then $x_1x_2x_3$ = (100) and (110), respectively.

Let us find all test patterns for the SA1 and SA0 faults on x_3:

$df(x)/dx_3 = x_1 x_2 \oplus 1 = (x_1 x_2)'$.

Let us equate its products with x_3 and x_3' to 1.

The patterns to detect the faults SA0 and SA1 are $x_3 (x_1 x_2)' = 1$ and $x_3' (x_1 x_2)' = 1$.

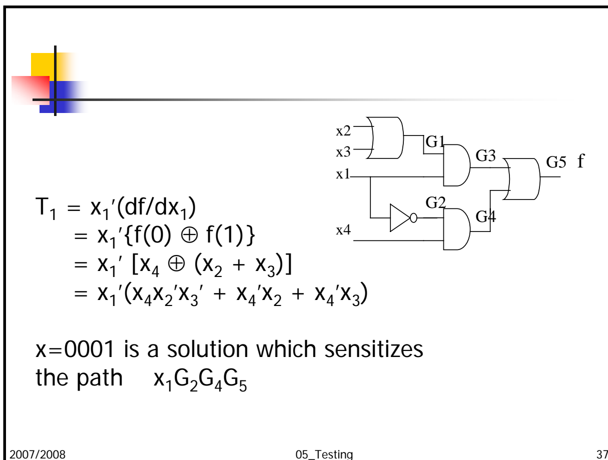
For the SA0, we must have

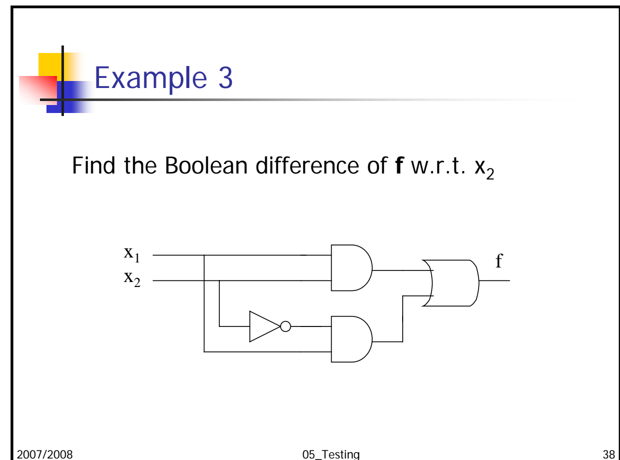
$x_3x'_1 + x_3x'_2 = 1$, i.e. x_1x_2x (001, 011, or 101)

For the SA1 we have $x_1x_2x_3$ = (000, 010, or 100)

Example 2

Find set of tests for x_1 SA1 in the circuit





$$f(x) = x_1x_2 + x_1\bar{x}_2$$

$$\frac{df}{dx_2} = f(0) \oplus f(1) = x_1 \oplus x_1 = 0$$

$$T_0 = x_2\frac{df}{dx_2} = 0$$

$$T_1 = \bar{x}_2\frac{df}{dx_2} = 0$$

Not testable

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Boolean difference w.r.t. an internal line

Theorem :
The set of all tests which detect h SA0 is defined by :

$$T_0 = h(x)\frac{df(x,h)}{dh}$$

and h SA1 is defined by:

$$T_1 = \bar{h}(x)\frac{df(x,h)}{dh}$$

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